深圳市天广宽科技有限公司

ShenZhen TGK Technology Co.,LTD

TM12864D-1　V1.0

(Liquid Crystal Display Module)

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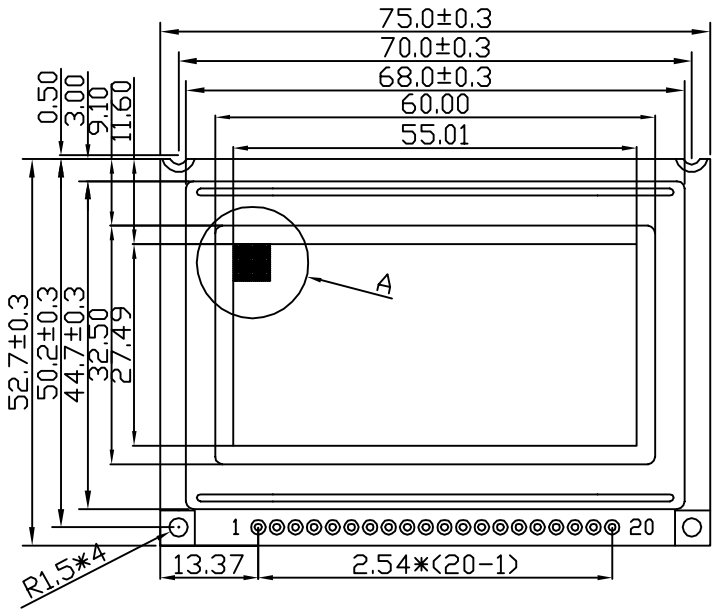
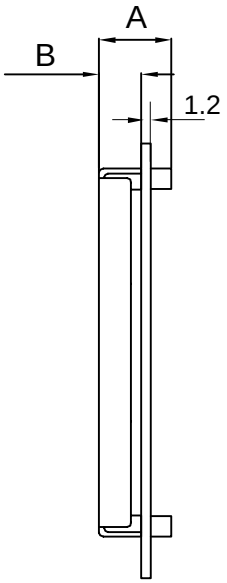
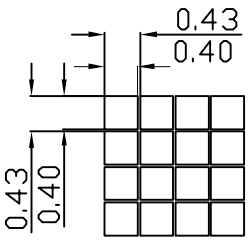
CONTENTS

➢ Mechanical diagram





A	B
MAX7.0	3.3 低框
MAX8.8	5.7 中框
MAX12.0	8.5 高框



Disply Format
128× 64DOTS
Drlvlng Merhod
1/64 Duty
1/9 Bais

➢ Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage for logic	Vdd - Vss	0	6.5	V
Input voltage	Vin	0	Vdd	
Operating temperature range	T0p	-20	70	℃
Storage temperature range	Tst	-25	75	

➢ Interface pin connections

Pin No.	Symbol	Level	Description
1	Vdd	3.3V--5.0V	Supply voltage for logic and LCD (+)
2	Vss	0V	Ground
3	V0	-	Operating voltage for LCD (variable)
4~11	DB0~DB7	H/L	Data bit 0~7
12	CS2	L	Chip select signal for IC2
13	CS1	L	Chip select signal for IC1
14	/RES	L	Reset signal
15	R/W	H/L	H: read (MUP<－module),L: write (MPU－>module)
16	D/I	H/L	H: data, L: instruction code
17	E	H, H L	Chip enable signal
18	VEE	-	Operating voltage for LCD (variable)
19	A	3.3V--5.0V	Backlight power supply
20	K	0V	Backlight power supply

➢ Optical characteristics

STN Type display module (Ta=25℃, Vdd=5.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	Cr≥2	-60	-	35	deg
	ϕ		-40	-	40	
Contrast ratio (rise)	Cr		-	6	-	
Response time (fall)	Tr	-	-	150	250	ms
	Tr	-	-	150	250	ms

➢ Electrical characteristics

Item		Symbol	Condition	Standard value			Unit
				Min.	Typ.	Max.	
Supply voltage for	Logic	Vdd - Vss	-	4.75	5.0	5.25	V
	LCD	Vdd-V0	-	-	9.5	-	
Supply current for	Logic	Idd	-	-	2.5	-	mA
	LCD	Iee	-	-	1.0	-	
Operating voltage for LCD (Recommended)		Vdd-v0	-	-	-	-	V
			25℃	-	9.5	-	
			-	-	-	-	
Input voltage	H: level	Vih	High level	0.7Vdd	-	Vdd	
	L: Level	Vil	Low level	0	-	0.3Vdd	

Electrical Absolute Maximum Ratings (KS0107B)

Parameter	Symbol	Rating	Unit	Note
Operating voltage	V_{DD}	-0.3 ~ +7.0	V	*1
Supply voltage	V_{EE}	V_{DD}-19.0 ~ V_{DD}+0.3	V	*4
Driver supply voltage	V_B	-0.3 ~ V_{DD}+0.3	V	*1,2
	V_{LCD}	V_{EE}-0.3 ~ V_{DD}+0.3	V	*3,4

***Notes:**

*1. Based on V_{SS} = 0V

*2. Applies to input terminals and I/O terminals at high impedance. (Except V0L, V1L, V4L, and V5L)

*3. Applies to V0L, V1L, V4L, and V5L.

*4. Voltage level: $V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

DC Electrical Characteristics (KS0107B)

(VDD= 4.5 to 5.5V, VSS=0V,VDD-VEE=8~17V,Ta= -30 to +85℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	V_{DD}	-	4.5	-	5.5	V	
Input voltage	V_{IH}	-	0.7_{VDD}	-	V_{DD}		*1
	V_{IL}	-	V_{SS}	-	$0.3V_{DD}$		
output voltage	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	-		*2
	V_{OL}	I_{OL}= 0.4mA	-	-	0.4		
Input leakage current	I_{LKG}	V_{IN}= V_{DD} ~ V_{SS}	-1.0	-	+1.0	μA	*1
OSC Frequency	fosc	Rf=47kΩ±2% Cf=20pF±5%	315	450	585	kHz	
On Resistance (Vdiv-Ci)	R_{ONS}	V_{DD}-V_{EE}=17V Load current±150μA	-	-	1.5	kΩ	
Operating current	I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	*3
	I_{DD2}	Master mode 1/128 Duty	-	-	0.2		*4
Supply Current	I_{EE}	Master mode 1/128 Duty	-	-	0.1		*5
Operating	f_{op1}	Master mode External Duty	50	-	600	kHz	
Frequency	f_{op2}	Slave mode	0.5	-	1500		

Notes

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M, and CL2 in the input state.

*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M, and CL2 in the output state.

*3. This value is specified about current flowing through V_{SS}.

Internal oscillation circuit: Rf=47kΩ, cf=20pF

Each terminals of DS1, DS2, FS, SHL, and MS is connected to V_{DD} and out is no load.

*4. This value is specified about current flowing through V_{SS}.

Each terminals is DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD},MS is connected to V_{SS} and CL2, M, DIO1 is external clock.

*5. This value is specified about current flowing through V_{EE}, Don't connect to V_{LCD}(V1~V5).

Electrical Absolute Maximum Ratings (KS0108B)

Parameter	Symbol	Rating	Unit	Note
Operating voltage	V_{DD}	-0.3 ~ +7.0	V	*1
Supply voltage	V_{EE}	V_{DD}-19.0 ~ V_{DD}+0.3	V	*4
Driver supply voltage	V_B	-0.3 ~ V_{DD}+0.3	V	*1,3
	V_{LCD}	V_{EE}-0.3 ~ V_{DD}+0.3	V	*2

***Notes:**

*1. Based on V_{SS} = 0V
*2. Applies the same supply voltage to V_{EE}. $V_{LCD}=V_{DD}-V_{EE}$.
*3. Applies to M, FRM, CLK1, CLK2, CL, RESETB, ADC, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.
*4. Applies V0L, V2L, V3L and V5L.

Voltage level: $V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

DC Electrical Characteristics (KS0108B)

(VDD= 4.5 to 5.5V, VSS=0V,VDD-VEE=8~17V,Ta= -30 to +85℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	V_{DD}	-	4.5	-	5.5	V	
Input High voltage	V_{IH1}	-	0.7_{VDD}	-	V_{DD}		*1
	V_{IH2}	-	2.0	-	V_{DD}		*2
Input Low voltage	V_{IL1}	-	0	-	$0.3V_{DD}$		*1
	V_{IL2}	-	0	-	0.8		*2
Output High Voltage	V_{OH}	I_{OH}= -0.2mA	2.4	-	-		*3
Output Low Voltage	V_{OL}	I_{OL}= 1.6mA	-	-	0.4		*3
Input leakage current	I_{LKG}	$V_{IN}= V_{SS} \sim V_{DD}$	-1.0	-	+1.0	μA	*4
Three-state (OFF) Input Current	I_{TSL}	$V_{IN}= V_{SS} \sim V_{DD}$	-5.0	-	5.0		*5
Driver Input leakage current	I_{DIL}	$V_{IN}= V_{EE} \sim V_{DD}$	-2.0		2.0		*6
On Resistance (Vdiv-Ci)	R_{ONS}	$V_{DD}-V_{EE}$=15V Load current±100μA	-	-	7.5	kΩ	*8
Operating current	I_{DD1}	During Display	-	-	0.1	mA	*7
	I_{DD2}	During Access Access Cycle=1MHz	-	-	0.5		*7

Notes

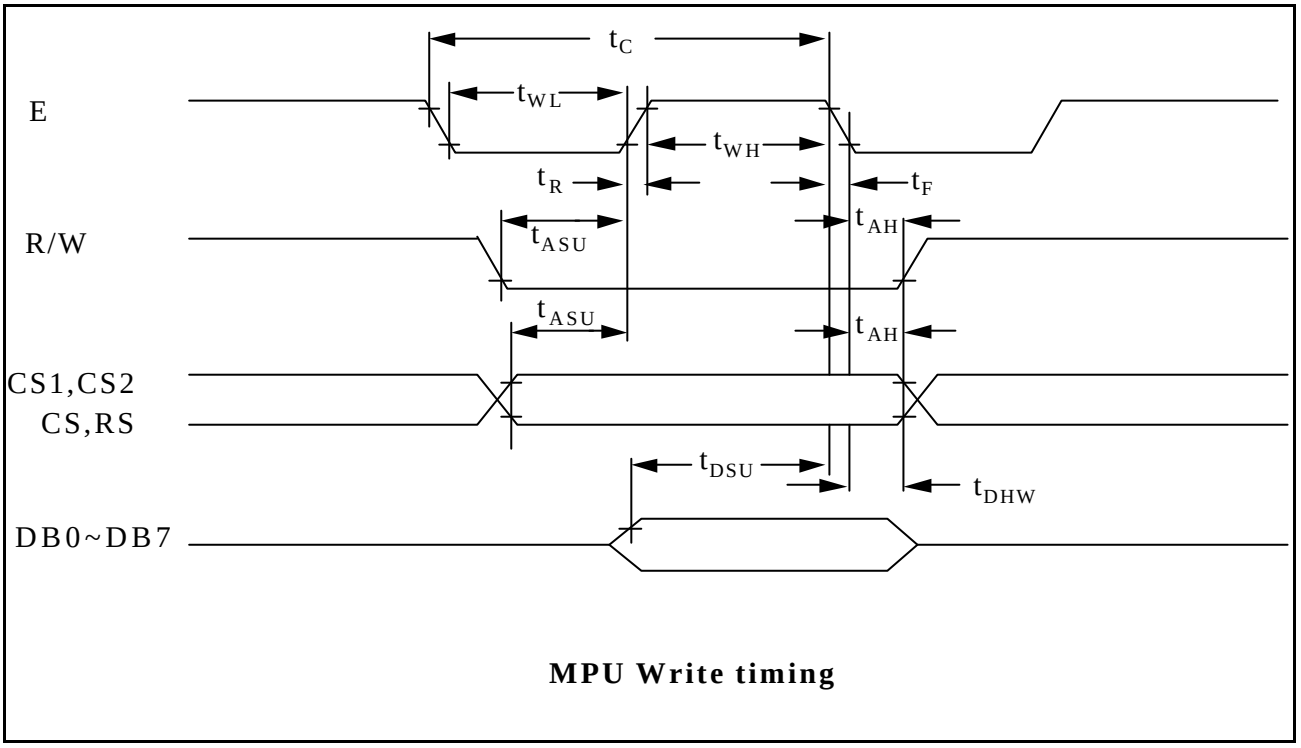
*1. CL, FRM, M, RSTB, CLK1, CLK2
*2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
*3. DB0~DB7
*4. Except DB0~DB7
*5. DB0~DB7 at high impedance
*6. V0, V1, V3, V3, V4, V5
*7. 1/64 duty, FCLK=250KHZ, Frame Frequency=70HKZ, Output: No Load
*8. $V_{DD}-V_{EE}$=15.5V

V0L>V2L>= V_{DD}-2/7($V_{DD}-V_{EE}$)>V3L= V_{EE}+2/7($V_{DD}-V_{EE}$)>V5L

➢ Write or read cycle

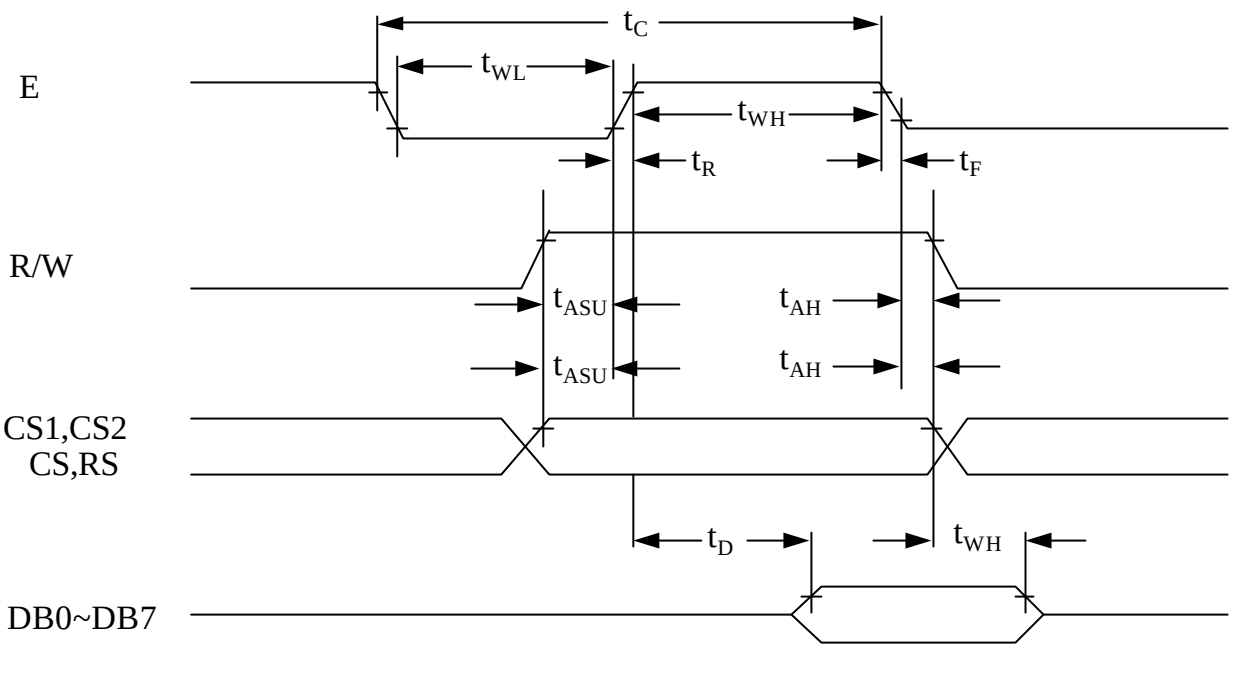
Characteristic	Symbol	Min.	Typ.	Max.	Unit
E cycle	Tc	1000	-	-	ns
E high level width	Twh	450	-	-	ns
E low level width	Twl	450	-	-	ns
E rise time	Tr	-	-	25	ns
E fall time	Tf	-	-	25	ns
Address set-up time	Tasu	140	-	-	ns
Address hold time	Tah	10	-	-	ns
Data set-up time	Tdsu	200	-	-	ns
Data delay time	Td	-	-	320	ns
Data hold time (write)	Tdhw	10	-	-	ns
Data hold time (read)	Tdhr	20	-	-	ns

✧ Write timing



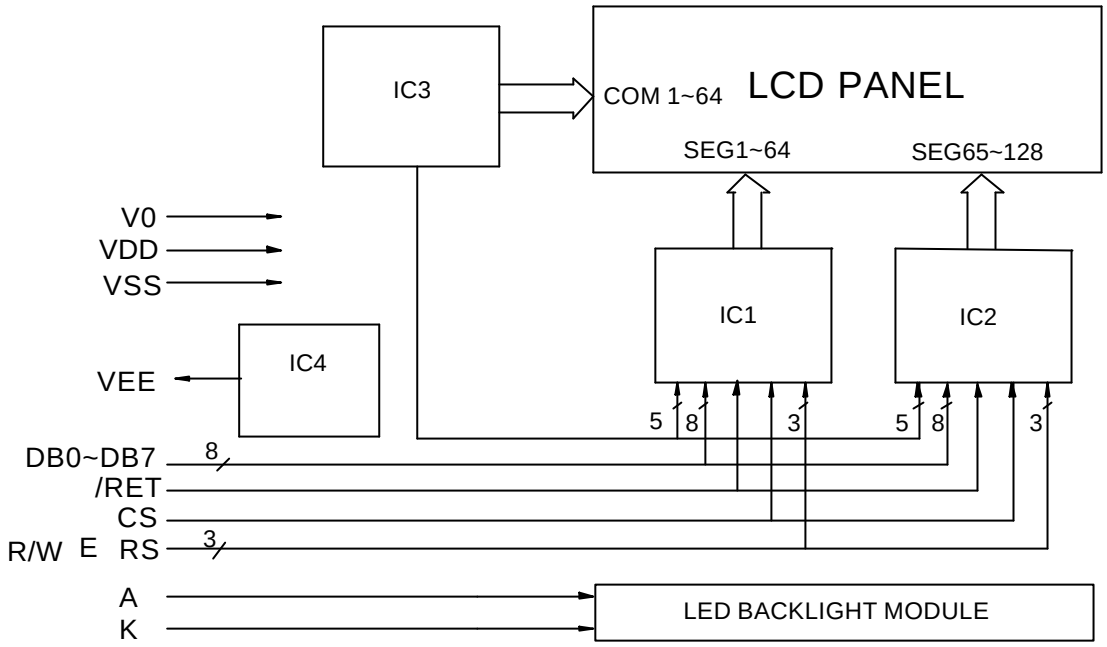
MPU Write timing

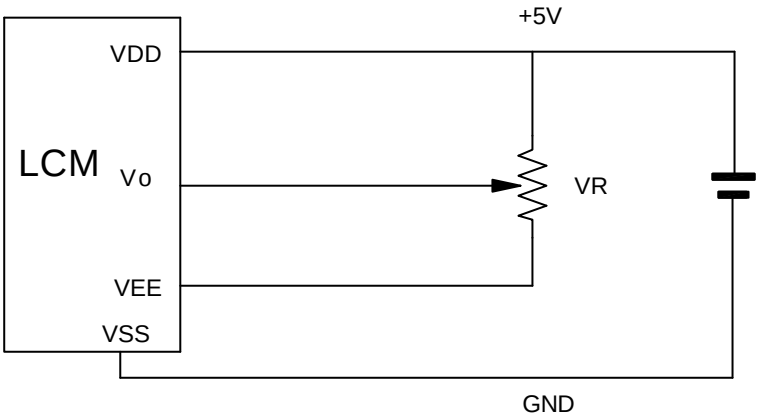
✧ Read timing



MPU Read timing

✧ Block diagram





VDD-Vo:LCD DRIVING VOLTAGE
VR:10K~20K

***Note**

1/64 duty, 1/9 bias

$V_{DD} \geqslant V1 \geqslant V2 \geqslant V3 \geqslant V4 \geqslant V5 \geqslant V_{EE}$

✧ Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read Display Data	1	1	Read data								Reads data (DB[7:0])from display data RAM to the data bus.
Write Display Data	1	0	Write data								Writes data (DB[7:0]) into display data RAM. After writing instruction, Y address is incriminated by 1 automatically
Status Read	0	1	Busy	0	ON/ OFF	Re-set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address in the Y address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

1. Display On/Off

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

2. Set Address (Y Address)

Y address (AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

3. Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

4. Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

7. Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

✧ Operating principles & methods

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS!B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.
When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H , RS=L, status data (busy check) can read out.
To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

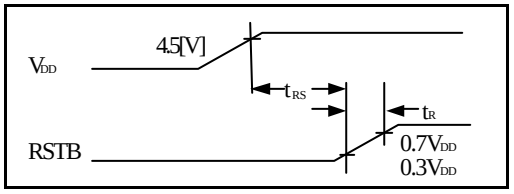
RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.
1. Display off
2. Display start line register become set by 0. (Z-address 0)
While RSTB is low, No instruction except status read can by accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction.
The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns

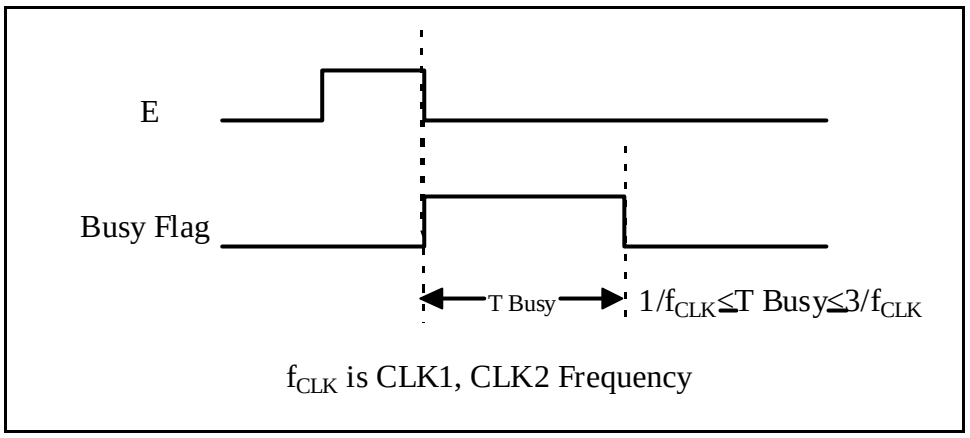


5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating .

When busy flag is low, KS0108B can accept the data or instruction.

DB7indicates busy flag of the KS0108B.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low.

The status of the flip-flop is output to DB5 by status read instruction.

The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.

Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or writes operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write datra1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H => Y-address 0: S1~Y address 63: S64

ADC=L => Y-address 0: S64~Yaddress 63: S1

ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.